Evaluation Board for 8-/16-Channel, 12-/14-Bit, Serial Input, Voltage-Output DACs

EVAL-AD5390/91/92EB

FEATURES

Full-featured evaluation board
On-board reference
On-board ADC for MON_OUT voltage readback
Link options
Direct hook-up to printer port of PC
PC software for control of DACs
Socketed AD539x for easy replacement

INTRODUCTION

This evaluation board is for the AD5390/AD5391/AD5392, 8-/16-channel, 12-/14-bit DACs. The AD539x parts contain 8/16, 12-/14-bit DACs in one package. They have a maximum output voltage span of 5 V derived from a reference voltage of 2.5 V.

The AD539x parts have a 2-wire I^2C interface and a 3-wire serial interface, which are compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The DAC outputs are updated when the DAC registers receive new data. All the outputs can be updated simultaneously by taking the $\overline{\text{LDAC}}$ input low.

Each channel has a programmable gain and offset adjust register. Each DAC output is gained and buffered on-chip.

See the AD5390/AD5391/AD5392 data sheet for product details.

AD539x EVALUATION BOARD POWER SUPPLIES

The following external supplies must be provided:

- 5 V between the DV_{CC} and DGND inputs for the digital supply of the AD539x.
- 5 V between the AV_{CC} and AGND inputs for the analog supply of the AD539x.

Both AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD539x. Avoid connecting AGND and DGND elsewhere in the system to avoid ground loop problems.

Each supply is decoupled to the relevant ground plane with 47 µF and 0.1 µF capacitors. Each device supply pin is again decoupled with a 10 µF and 0.1 µF capacitor pair to the relevant ground plane.

FUNCTIONAL BLOCK DIAGRAM

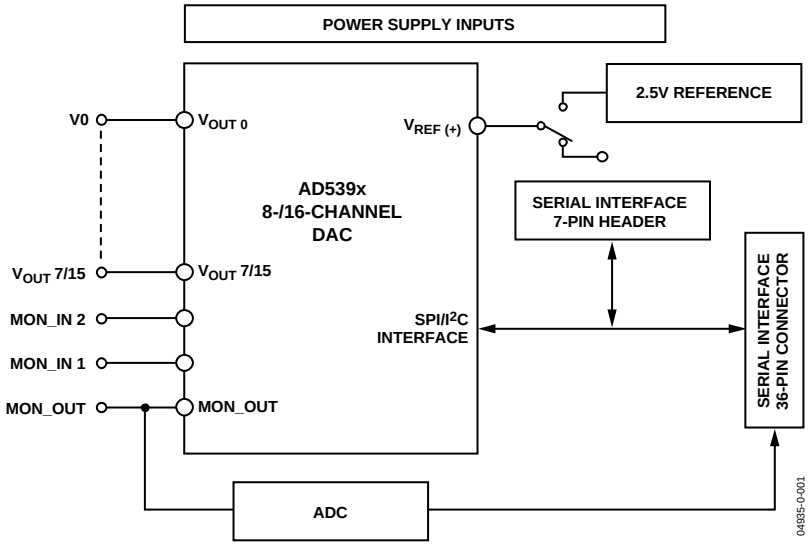


Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

7/04—Revision 0: Initial Version

LINK AND SWITCH OPTIONS

The link and switch options on the evaluation board should be set for the required operating setup before using the board. The functions of the link and switch options are described in Table 1.

Table 1. Link Options

Link/Switch No.	Function
LK1	For normal operation, this link should not be inserted.
	When this link is inserted, it connects the RESET pin to DGND, resetting the AD539x.
LK2	For normal operation, this link should not be inserted.
	When this link is inserted, it connects the CLR pin to DGND, clearing the outputs of the AD539x to the user-programmed value.
LK3	This link selects the state of LDAC.
	When inserted, $\overline{\text{LDAC}}$ is connected to DGND and , therefore, the DACs update automatically.
	When removed, $\overline{\text{LDAC}}$ is connected to DV_{CC} and must be brought low by the digital interface to update the DACs.
LK4	When this link is inserted, it connects the AV_{CC} pin of the AD539x to the MON_IN1 pin, so that the AV_{CC} value can be monitored using the on-board ADC.
LK5	When this link is inserted, it connects the reference pin of the AD539x to the MON_IN2 pin, so that the reference value can be monitored using the on-board ADC.
LK6	This pin selects the reference.
	Position A selects the externally applied reference at J4.
	Position B selects the on-board 2.5 V reference.
S1	This pin selects the power-down state.
	Position H powers down the AD539x.
	Position L removes the AD539x from power-down.
S2	This switch selects the interface.
	Position H selects the SPI interface.
	Position L selects the I^2C interface.
S3	In I^2C mode, this switch selects the state of the Address Bit A1.
	Position H sets A1 = 1.
	Position L sets A1 = 0.
	In SPI mode, this switch selects the state of daisy-chain mode.
	Position H enables daisy-chain mode.
	Position L disables daisy-chain mode.

LINK AND SWITCH OPTION SETUP FOR PC CONTROL

The PC controls the AD539x over the SPI interface, which must be enabled for PC control. The link and switch options for PC control are listed in Table 2.

Table 2. Link and Switch Options for PC Control

Link/Switch No.	State	Function
LK1	Removed	
LK2	Removed	
LK3	Removed	
LK4	Inserted	MON_IN1 Connected to AV_{CC}
	Removed	MON_IN1 Input from J2
LK5	Inserted	MON_IN2 Connected to Reference
	Removed	MON_IN2 Input from J2
LK6	A	External Reference Selected
	B	On-Board Reference Selected
S1	L	
S2	H	
S3	L	

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD5390/91/92EB evaluation kit includes self-installing software on CD-ROM. If the setup file does not run automatically, you can run setup.exe from the CD-ROM.

The evaluation board software is compatible with Windows® 95 to Windows XP. Ensure that the Centronics cable connects the PC to the EVAL-AD5390/91/92EB evaluation board.

1. On the Analog Devices menu, select **AD539x Evaluation Software**.
2. At the prompt, select the relevant device.

The **AD5390/91/92 Evaluation Software** dialog box is displayed. Figure 2 shows the drop-down menus (**File**, **Printer Port**, **Dac**, **Register**, and **Help**).

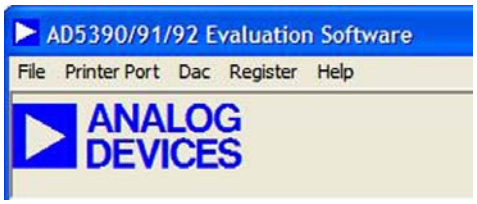


Figure 2.

LOAD DAC CHANNELS

The **Dac** menu allows user control of the 8/16 DAC channels, as well as other functions such as hardware reset of the DAC channels and clearing the outputs.

To load DAC channels:

1. On the **Dac** menu, select **Load/Calibrate Dac Channel**. The **Load/Calibrate Dac Outputs** dialog box is displayed.

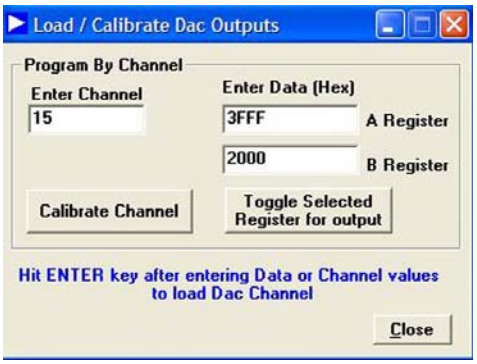


Figure 3.

2. In the **Enter Channel** box, enter the channel selection.
3. In the **Enter Data (Hex)** box, type a DAC code to load to the selected channel.
4. Press **Enter** on your keyboard after entering data.
5. Each DAC has two associated data registers, the A Register and the B Register. Click the **Toggle Selected Register for output** button to toggle between the two registers.

CHANNEL CALIBRATION

1. Click **Calibrate Channel** to display the **Channel Calibration** dialog box.

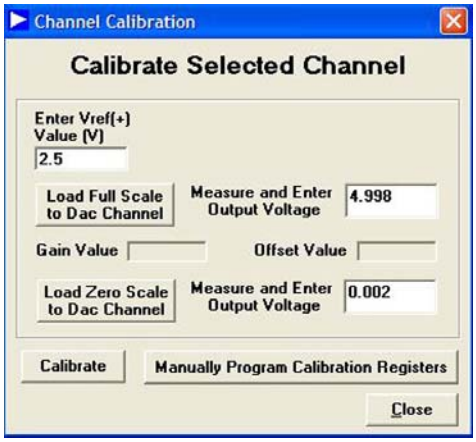


Figure 4.

2. Type the reference value in the **Enter Vref(+) Value (V)** box.
3. Load full scale and measure the output voltage on the relevant channel.
4. Input this value in the appropriate field in the dialog box.
5. Load zero scale and again enter the measured value in the appropriate field.
6. Click **Calibrate** to calibrate the device to the required output voltage.

You can also manually program the gain and offset registers.

1. Click **Manually Program Calibration Registers**. The **Program m and c Registers** dialog box is displayed.

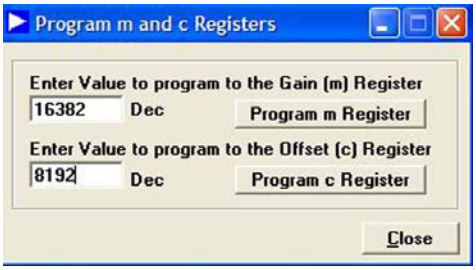


Figure 5.

2. Type values for the gain and offset registers and click the accompanying buttons to program the registers.

PROGRAM OUTPUT RANGE

You can reduce the output range of each DAC channel using the offset and gain registers. To access the **Output Range** dialog box, select **Program Output Range** from the **Dac** menu.

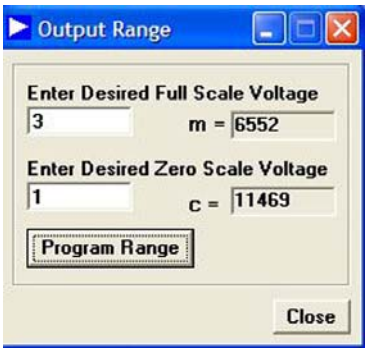


Figure 6.

1. Type the desired full-scale and zero-scale values in the appropriate boxes.
2. Click **Program Range**. The m and c registers are programmed with the displayed values, and the output range is set to the user-selected values.

SPECIAL FUNCTION REGISTER

The **Special Function Register** dialog box allows access to all the register functions. To access this dialog box, select **Special Function Register** from the **Register** menu.

Software Clear

The **Software Clear** area allows you to clear the DAC channels to a user-specified value:

1. If you want to clear the DAC channels to the user-specified value (default value is 0 V), click **Soft Clear**.
2. If you want to program the user-specified value, type the value in the **Enter Code** box and click **Write Code.**

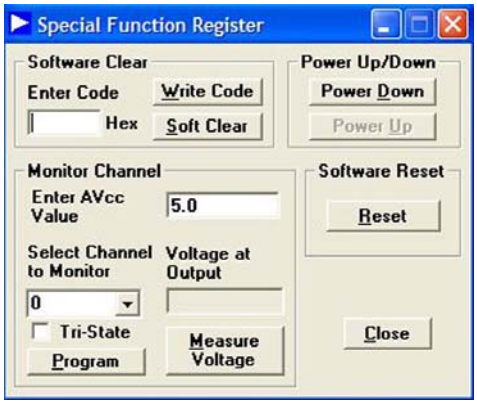


Figure 7.

Monitor Channel

The **Monitor Channel** area allows you to monitor the DAC channels via the MON_OUT pin. Before the monitor function can operate, you must enable it in the control register:

1. Type the AV_{CC} value in the **Enter AV_{CC} Value** box. This value is used as the reference for the on-board ADC.
2. Select the channel that you want to monitor in the **Select Channel to Monitor** box.
3. Optional: To three-state the MON_OUT pin, select the **Tri-State** check box.
4. Click **Program.**
5. To measure and display the voltage at the MON_OUT pin, click **Measure Voltage**.

Power Up/Down and Software Reset Functions

Click **Power Down**, **Power Up**, or **Reset**, as needed, to activate or deactivate these functions.

CONTROL REGISTER

To access the **Control Register** dialog box, select **Register** from the **AD5390/91/92 Evaluation Software** dialog box. The **Control Register** dialog box allows user access to all the control register functions. The current bit values of the control register are displayed in the **Contents of Control Register** area. Eight functions are available, as shown in Figure 8.

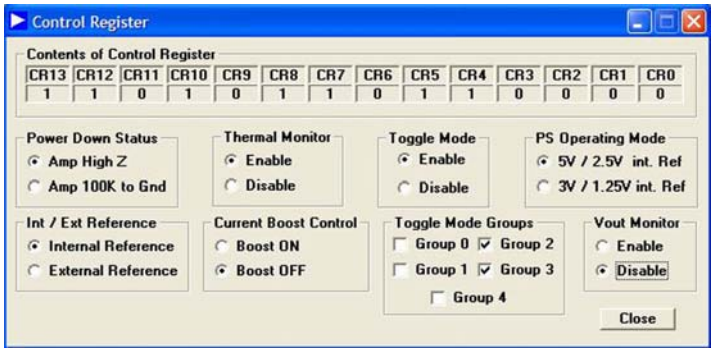


Figure 8.

COMPONENT LISTING

Table 3.

Qty	Reference Designator	Description	Supplier/Number
1	U1	AD539x	Analog Devices
1		64-Lead LFCSP Socket	Plastronics 64QN50T19090-J
1	U2	AD780	Analog Devices
1	U3	AD7476ART	Analog Devices
4	R1–R4	10k Resolution (0805 Package)	FEC 911-975
10	C1–C6, C8–C10, C22	0.1 µF Multilayer Ceramic Capacitor (0603 Package)	FEC 499-675
5	C15–C19	10 µF Tantalum Capacitor (TAJ-A Package)	FEC 197-130
4	C11–C14	470 pF X7R Ceramic Capacitor (0603 Package)	FEC 498-580
1	C7	10 nF X7R Ceramic Capacitor (0603 Package)	FEC 499-146
2	C20, C21	47 µF Tantalum Capacitor (TAJ-C Package)	FEC 197-324
1	J1	36-Lead Centronics Connector (IEEE 488 Style)	FEC 147-753
1	J2	Header 20	FEC 148-195
7	J4–J10	Gold 50 Ω SMB Jack	FEC 310-682
1	J3	Header 07	FEC 512-084
2	J12, J14	Black Banana Socket	FEC 150-040
2	J11, J13	Red Banana Socket	FEC 150-039
5	LK1–LK5	Header (2 × 1 pin)	FEC 511-705
1	LK6	Header (3 × 1 pin)	FEC 511-717
3	S1–S3	Header (3 × 1 pin)	FEC 511-717

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

EVALUATION BOARD SCHEMATICS

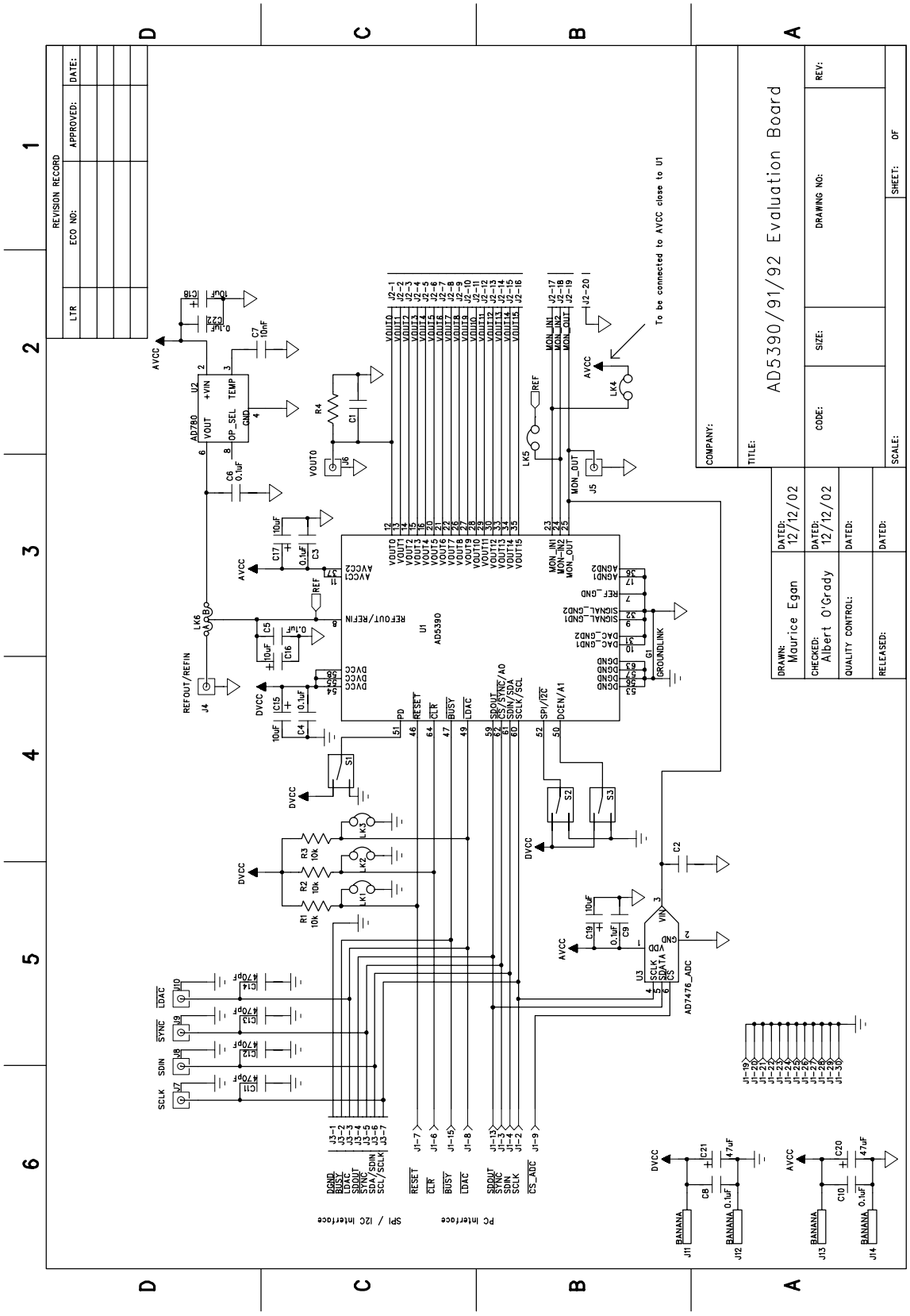


Figure 9.

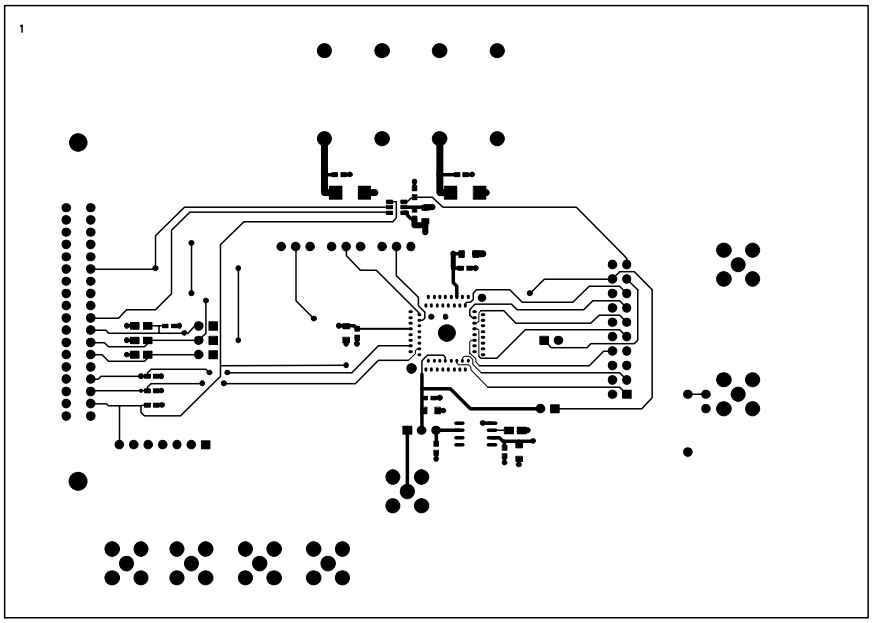


Figure 10.

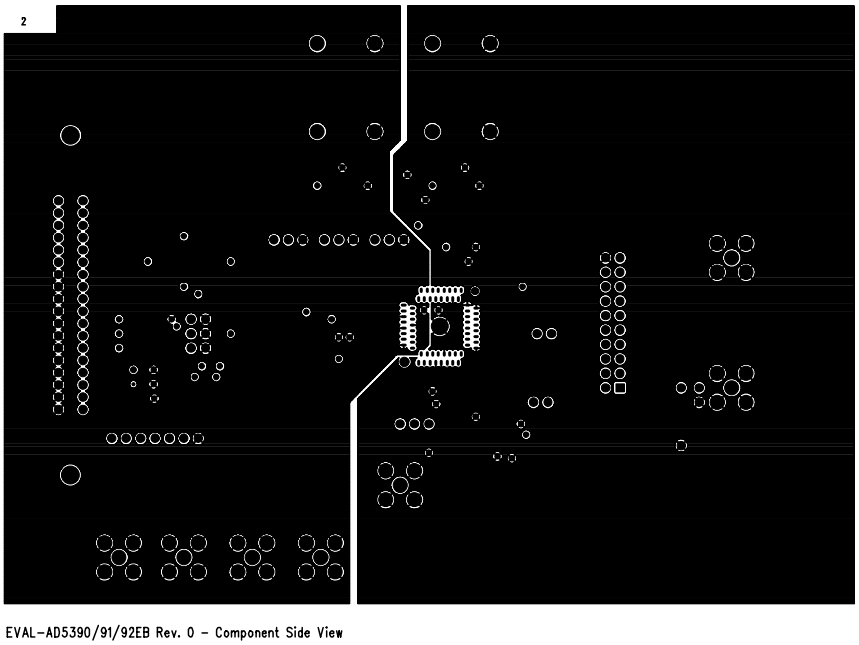
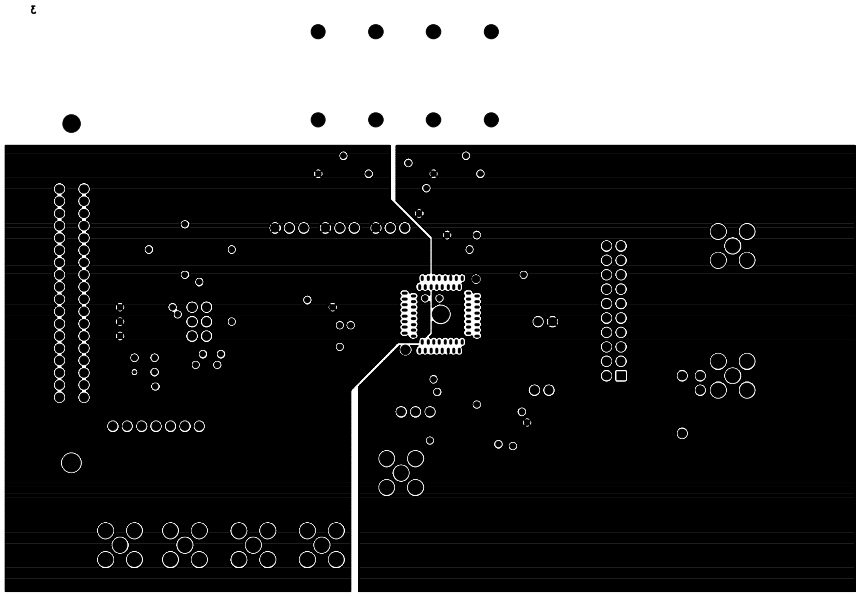


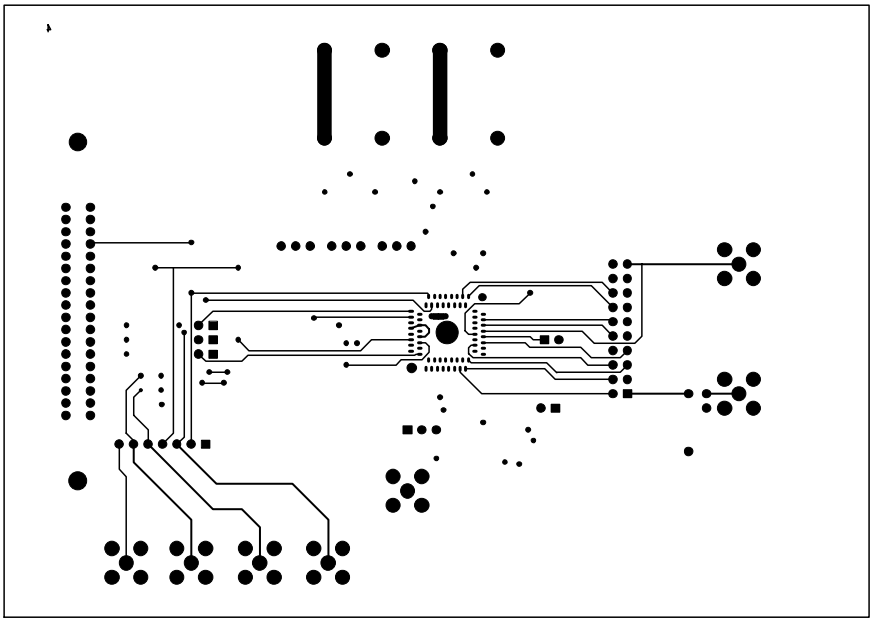
Figure 11.



EVAL–AD5390/91/92EB Rev. 0 – Component Side View

04935-0-012

Figure 12.



EVAL–AD5390/91/92EB Rev. 0 – Component Side View
Solder Side Artwork

04935-0-013

Figure 13.

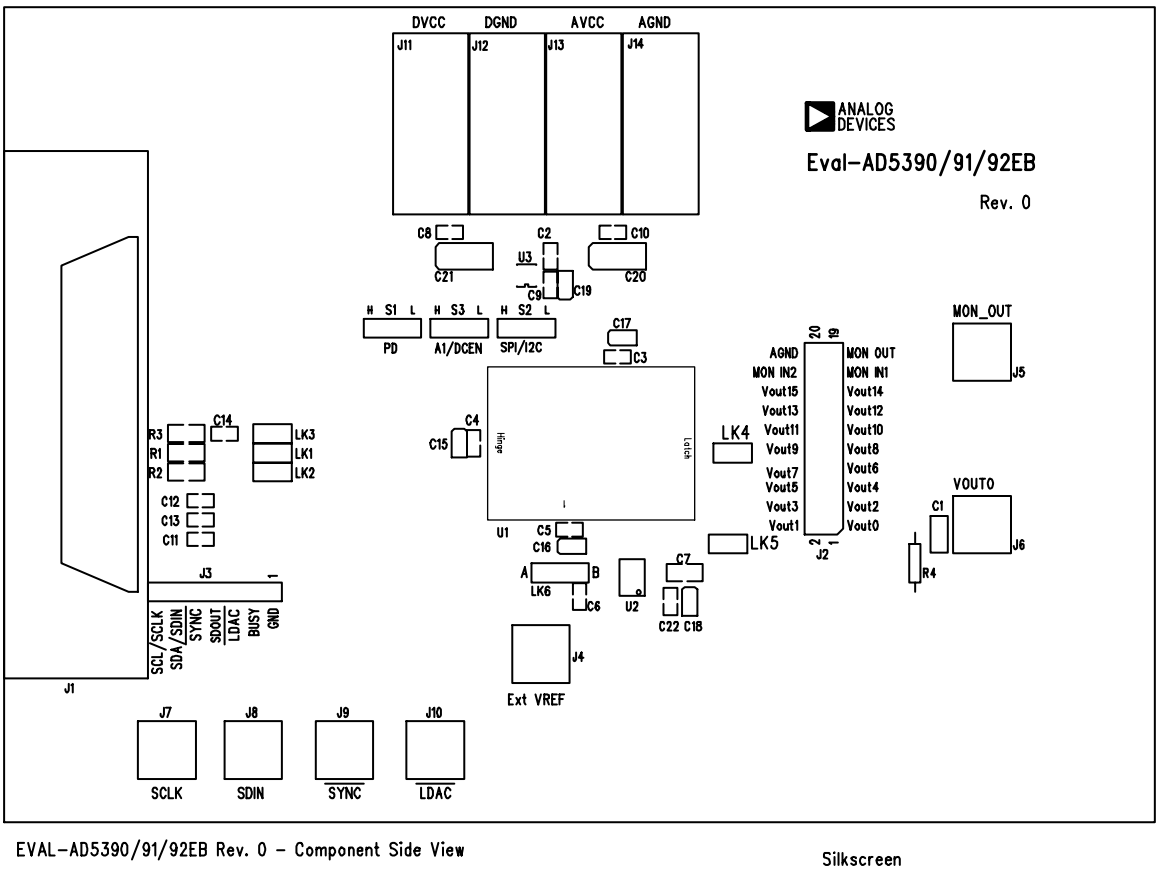

DVCC
DGND
AVCC
AGND
J11
J12
J13
J14
ANALOG DEVICES
Eval-AD5390/91/92EB
Rev. 0
C8
C21
C2
U3
C9
C19
C10
C20
H S1 L
PD
H S3 L
A1/DCEN
H S2 L
SPI/I2C
C17
C3
C4
C15
C14
R3
R1
R2
LK3
LK1
LK2
C12
C13
C11
U1
C5
C16
LK4
LK5
AGND
MON IN2
Vout15
Vout13
Vout11
Vout9
Vout7
Vout5
Vout3
Vout1
MON OUT
MON IN1
Vout14
Vout12
Vout10
Vout8
Vout6
Vout4
Vout2
Vout0
J2
MON_OUT
J5
VOUT0
C1
J6
R4
J3
SCL/SCLK
SDA/SDIN
SYNC
SDOUT
LDAC
BUSY
GND
J1
A
B
LK6
C6
U2
C7
C22
C18
J4
Ext VREF
J7
J8
J9
J10
SCLK
SDIN
SYNC
LDAC
EVAL-AD5390/91/92EB Rev. 0 - Component Side View
Silkscreen
04935-0-014

Figure 14.

ORDERING GUIDE

Model	Package Description
EVAL-AD5390EB	AD5390 Evaluation Board Kit
EVAL-AD5391EB	AD5391 Evaluation Board Kit
EVAL-AD5392EB	AD5392 Evaluation Board Kit

D04935–0–7/04(0)